Utkarsh Gupta

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Summary

Computer Engineering PhD candidate focusing on hardware verification and synthesis.

- Understanding of EDA flow (specification, synthesis, verification, layout).
- Knowledge of formal hardware verification techniques.

Education

- **PhD Candidate, Computer Engineering, University of Utah** **GPA: 3.97** **2014 - Present**
  - Research Focus: Formal hardware verification and rectification using computational algebraic geometry
  - Advisor: Dr. Priyank Kalla
- **B.Tech, Electronics and Communication Engineering, Tezpur University, India** **CGPA: 9.46/10** **2014**
  - Tezpur University B.Tech merit based scholarship

Experience

- **Graduate Intern** **Apple Inc., Portland** **Summer 2019**
  - Planned, developed, and executed FV on RTL design which is part of error handling in Apple microprocessor cache.
  - FV environment provided high confidence on correctness of relevant logic and resulted in interesting corner case bugs discoveries in the early stage of design cycle.
- **Graduate Technical Intern** **Intel Corporation, Hillsboro** **Summer 2018**
  - Gained hands-on experience verifying System Verilog RTL designs using state of the art FV tools and methodology.
  - Developed a formal verification plan and used it for verifying floating point arithmetic components of Intel AI Processors.
  - Formally verified industrial grade FIFO to be used in Intel's next generation High Performance Computing Chips.

Publications

- **Utkarsh Gupta**, Priyank Kalla, Irina Ilioaea, Florian Enescu, "*Exploring Algebraic Interpolants for Rectification of Finite Field Arithmetic Circuits with Groebner Bases*", ETS, May 2019
- **Utkarsh Gupta**, Irina Ilioaea, Vikas Rao, Arpitha Srinath, Priyank Kalla, Florian Enescu, "*On the Rectifiability of Arithmetic Circuits using Craig Interpolants in Finite Fields*", VLSI-SoC, Oct 2018
- Vikas Rao, **Utkarsh Gupta**, Irina Ilioaea, Arpitha Srinath, Priyank Kalla, Florian Enescu, *"Post-Verification Debugging and Rectification of Finite Field Arithmetic Circuits using Computer Algebra Techniques"*, FMCAD, Oct 2018
- **Utkarsh Gupta**, Irina Ilioaea, Priyank Kalla, Florian Enescu, Vikas Rao, Arpitha Srinath, *"Craig Interpolants in Finite Fields using Algebraic Geometry: Theory & Application"*, International Workshop on Logic & Synthesis, June 2018
- **Utkarsh Gupta**, Priyank Kalla, Vikas Rao, *"Boolean Grobner Basis Reductions on Finite Field Datapath Circuits using the Unate Cube Set Algebra"*, IEEE Transactions on CAD, March 2018.

Software Tool Skills

- **Programming Languages:** C, C++, Verilog, VHDL, Python, Assembly, BASH, TCL
- **Hardware Verification /Design:** ABC, Boolector, VIS, Z3, Cadence Virtuoso, Synopsys Design Compiler, SPICE, ESPRESSO, SIS
- **Other:** Singular, LaTeX, Git, CUDD, Modelsim, MATLAB, PolyBori

Academic and Engineering Skills

- **Hardware Verification**
  - Computer algebra and algebraic geometry based formal hardware verification using symbolic computation.
    - Polynomial rings, finite fields, ideals, varieties, Groebner basis, and Hilbert's Nullstellansatz
  - Graph based verification using BDDs and AIGs
  - Equivalence checking using miters and SAT/SMT tools
- **Hardware Design and Synthesis**
  - Digital VLSI CMOS cell library design
  - Physical design automation techniques
  - Analysis of circuit timing and performance
  - Processor architecture design, pipelining, and cache designs

Other Projects

- **Synthesis of a Seven-Segment Display Driver**
  - Implemented a design for a Seven-Segment display driver that can control eight such segments and uses SPI protocol.
  - Performed synthesis and layout of the module with a custom-made library using Cadence Virtuoso, Synopsys design compiler, Cadence SoC Encounter.
- **Detecting Spam YouTube Comments**
  - Performed feature extraction and applied Perceptron, Support Vector Machines, Naive Bayes, and Multilayer Perceptron classifiers achieving a maximum accuracy of 93%.
- **Two-level hazard-free logic minimizer**
  - Implemented efficient algorithms for exact two-level hazard-free logic minimization for asynchronous circuits using python.
  - Implementation targets minimization for two-level standard gates and takes an extended burst-mode machine as input.