

# **Micron Engineering Clinic Project Proposal**

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## **Abstract**

This paper presents a cost-effective and accurate statistical analysis of a high speed chip-to-chip communication link. Implemented in graphical user interface this tool will read data from an outside source and output the resulting performance diagram, pass/fail, and bit error rate on a user-defined basis. The software tool will use mathematical models to characterize the performance of a high speed chip-to-chip interconnect. This software tool will include multiple sources of co-channel interference and transmitter/receiver jitter. The goal is to produce an output of simulated results that match real world applications to help understand if a design is valid.

## **Introduction**

In modern high performance computing systems, memory access is a major bottleneck. A single access to main memory can take hundreds of clock cycles. To a degree, modern cache and out-of-order processor architectures get around this by exploiting locality and instruction-level parallelism. However, accesses to off-chip memory are inevitable. Designing fast chip-to-chip interconnects is critical in reducing this bottleneck.

However, high-frequency chip-to-chip communication introduces signal degradation and limits the maximum achievable data-rates. Some of the issues encountered with chip to chip communication are jitter, signal noise, and reference voltage noise. Many of these problems are caused by channel impact on the analog signals used to represent bit values at high frequencies. Other problems result from timing uncertainty in clocking, causing clock jitter, which makes sampling correct bit values more difficult. There are several methods used for dealing with these problems. This project will focus on calculating the worst possible outcome and a statistical approach to verification of interconnect designs.

To ensure that these issues do not result in intolerable bit error rates, it is important to calculate all the possible sources of error and add them together in an attempt to validate a working design before fabrication. Traditionally this has been done by running a model of the design many times

and plotting the results over one period of time. This plot is called an eye-diagram. Running a model of the design many times can be problematic and time consuming for complex designs. By calculating an overall worst performance scenario an interconnect design can be validated for a given sampling window. The worst-case scenario is a condition that may occur but will not reflect the systems overall performance. Identifying this condition requires running the system model exhaustively. It is possible, however, to calculate this condition using mathematical models and then summing all the results. One of the goals of this project is to capture this mathematical model in a software based tool to expedite the verification process.

An eye-diagram can also be generated using a statistical approach. Using a statistical model it is possible to calculate the bit error rate under normal operating conditions. This is in contrast to the worst case method which assumes conditions that will not normally occur. A Gaussian distribution is used for the probability density function (PDF) of the ideal voltage of both a digital “one” and “zero”. The probability of error due to voltage uncertainty can be calculated mathematically. This determines the height of the statistical eye-diagram. A similar scheme is used to determine the width of the statistical eye-diagram. A Gaussian distribution is used for the PDF of the timing uncertainty caused by jitter from the transition from a one to a zero or a zero to a one in the data signal. The statistical analysis shows a probabilistic data eye diagram of error due to simultaneous voltage and timing uncertainty. This is useful because it is a more realistic analysis of the bit error rate of a high speed interconnect.

It is proposed that a software tool be developed to use these techniques to assist the validation of interconnect designs. The tool will be cross platform and will utilize a graphical user interface. The tool will read in data from HSpice, and will allow the user to select a statistical or worst-case analysis of the signals. The tool will then display the resulting eye diagram and related information. The tool should also allow for the user to define inputs such as transmitter/receiver jitter and co-channel interference.

This proposal is laid out as follows: First, a technical background of the problems involved in designing a model for high speed interconnects. Second, a detailed description of the work proposed to help overcome these problems. Third, an outline of the tasks involved in this project and their corresponding completion dates. It concludes with a summary of what is hoped to be accomplished by this effort.

## **Background**

There are several limiting factors in the design of high speed interconnects. These factors include:

### *Jitter*

Jitter is an unwanted variation of a periodic signal which degrades the performance of high-speed I/O links by limiting the maximum achievable data-rates. Transitions in both the clock and data stream introduce jitter into the receiver.

### *Noise*

Noise is the fluctuation in and the addition of external factors to the data stream, which can cause problems in interpretation of digital ones and zeros. Noise occurs in both the reference voltage and the signal itself. The figure below shows an eye-diagram with jitter and noise present.

### *Intersymbol Interference*

Intersymbol Interference (ISI) is a form of distortion of a signal in which one symbol interferes with subsequent symbols.

### *Channel*

The channel itself can have an impact on the signal. At high frequencies, the channel acts like a transmission line. The inherent resistance and capacitance of the channel act as a filter, distorting the amplitude and phase of the signal.

These limiting factors can be modeled mathematically and by using a pulse based analysis we can calculate their effects. To make information useful, the worst-case and statistical signal analysis methods described in the introduction must be used.

## **Proposed Work**

It is proposed that a CAD tool be developed which implements the worst-case and statistical methods. Several baseline and additional requirements have been established for this tool. The baseline requirements are as follows:

- Will provide a cross-platform GUI
- Will read in data from HSpice
- Will allow user to select Worst-Case or Statistical
- Will provide visualization of resulting eye diagrams
- Will allow for multiple sources of co-channel interference
- Will allow for user defined transmitter and receiver jitter
- Will output a pass/fail status based on worst-case analysis
- Will output a BER based on Statistical analysis

The additional requirements are not so clearly defined and their implementation will largely depend on available time. Some of these include incorporation of a user-defined transmitter FIR filter and output of a worst-case bit pattern based on a pulse response. This work is to be accomplished in the following manner.

First, to ensure proper understanding of the problems listed a prototype of the worst-case and statistical analysis methods will be done in Matlab. Given these prototypes it will be easier to ensure correctness in the final implementation. Second, JAVA will be used to design a cross-platform GUI to implement the HSpice file parser, worst-case and statistical analysis sections. JAVA was chosen because it provides a massive standard library containing functions that will be useful in performing the necessary math, plotting, file I/O, and GUI functionality. JAVA is also portable to any system that has the JAVA Virtual Machine installed correctly. Lastly, the code will be thoroughly tested and documented for use by engineers. If time permits, some/all of the additional features will be implemented.

### **Tasks and Time-line**

The completion of this proposed work will break down into the following tasks with their respective completion dates:

1. Plotting code December 13th 2008
2. Spice simulations December 13th 2008
3. Worst-case code January 6th 2009
4. Worst-case/Statistical Implementation (Matlab) January 10th 2009
5. Statistical code January 10th 2009
6. Worst-case ported January 17th 2009
7. Statistical ported January 20th 2009
8. File I/O January 24th 2009
9. GUI view January 27th 2009
10. JAVA GUI/File IO & Port Matlab January 31st 2009
11. Controller/Event handler January 31st 2009
12. Debug & Bonus Deliverables February 28th 2009
13. Final Presentation & Documentation March 31st 2009

### **Summary**

This paper outlines the worst-case and statistical analysis methods presented in [1] and [2]. It also proposes the development of a CAD tool. This CAD tool will implement the worst-case and statistical analysis methods to provide engineers with an accurate method for validation of interconnect designs. Currently, there are no commercially available tools that correctly perform all tasks that this work proposes to accomplish. It is expected that the result of this effort will provide interconnect designers with the necessary signal analysis resources to design faster interconnects with acceptable bit-error ratios.